Instruction:

Complete all questions in 1 hour.

1. Which one is the characteristic of Harvard Architecture?
2. **Program and Data stored in Separate Memory**
3. Program and Data stored in the same Memory
4. Program and data stored in Cache Memory
5. All of the Above
6. Which of the following is the working cycle of the CPU?
7. Decode, Execute, Fetch
8. **Fetch, Decode, Execute**
9. Fetch, Execute, Decode
10. All of the Above
11. Any condition that causes a processor to stall is called \_\_\_\_\_\_\_\_\_
12. **Hazard**
13. Page fault
14. System error
15. None of the mentioned
16. What does the control unit generate to control other units?
    1. Transfer signals
    2. Command Signal
    3. **Control signals**
    4. Timing signals
17. What must the processors of all computers have?
    1. Control unit
    2. ALU
    3. Register
    4. **All of these**
18. Which is the fastest memory in the computer?
19. **Cache**
20. RAM
21. Register
22. Hard disk
23. With the help of \_\_\_\_\_\_\_, we reduce the memory access time:
    1. SDRAM
    2. **Cache**
    3. Heaps
    4. Higher capacity RAMs
24. For a given FINITE number of instructions to be executed, which architecture of the processor provides for a faster execution?
    1. ISA
    2. ANSA
    3. **Super-scalar**
    4. All of the mentioned
25. A processor performing fetch or decoding of different instruction during the execution of another instruction is called \_\_\_\_\_\_
    1. Super-scaling
    2. **Pipe-lining**
    3. Parallel Computation
    4. None of the mentioned
26. A 24 bit address generates an address space of \_\_\_\_\_\_ locations.
    1. 1024
    2. 4096
    3. 248
    4. **16,777,216**
27. The USA contains about 3100 counties. Suppose you have a table that stores, for each county, its name (up to 40 characters in 8-bit ASCII), its state (a two-letter code), its population, and its median income (both as 32-bit numbers). How much space would the whole database take in memory?

Ans:

Space needed per row of the table:

Calculations

Name 40 Characters 40 bytes

State 2 Characters + 2 bytes

Population 32 bit integer + 4 bytes

(32 bits/8 bits/byte = 4 bytes)

Median Income 32 bit integer + 4 bytes

50 bytes

If there are 3100 rows, that means 3100 rows × 50 bytes/row = 155,000 bytes for the whole table. Finally,

155,000 bytes / 1024 bytes/binary KB ≈ 151.367 KB.

1. The computer has a maximum addressable memory of 16 Gigabytes. Its address bus width is 32.
2. Calculate the width of the data bus.

Total memory= 2 Address bus \*width of data bus

16GB=2 32 \*width

16\*2 30 =2 32 \*width [gb into byte, \*2 30]

2 4 \*2 30 \*2 3= 2 32 \*width [ into bits, \*2 3]

2 5= width

Width of the data bus =32 bits or 4 bytes

1. State the effect that adding one new line to the address bus would have on the maximum addressable memory.

Ans:

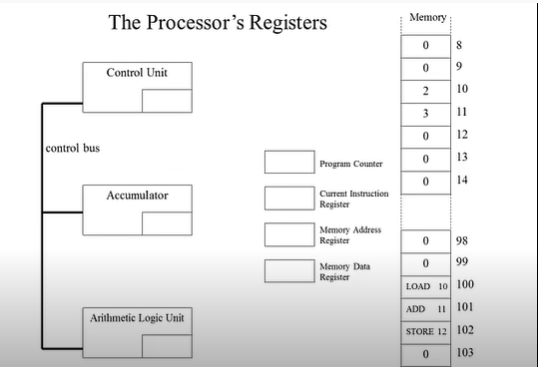
Here when adding a line in the address bus, it becomes 2 33 Thus, 2 4, or 16 bits or 2 bytes

1. Explain the *Instruction cycle* of the processor by taking an example of the program

Load: [10]

Add: [11]

Store: [12]



First, in the processor, LOAD10. Therefore, the value in the program counter (PC) will be processed to 100 as indicated in the memory instruction cycle. Then the memory address register registers the entry of PC address 100 and the memory data register registers LOAD10 then the current  
The instruction register stores the LOAD10 from the MDR. The memory value of 10 is 2 which is entered into the control device CU. 2 entries accumulator when transferred from CU. Then PC automatically changes or is added 1 so it is 101, so MAR address 101 and MDR register ADD11 as given in memory. The CU is commanded to fetch 3 depending on the memory. Since add is an arithmetic expression, it adds a CU (2+3) value of 5. Automatically addresses PC and MAR 102. CIR and MDR entries Store 12 as explained above. A memory value of 12 is entered into the accumulator. So this way the CPU's instruction cycle works.

1. Write short notes on the following topic:
2. Von Neumann and Harvard Architecture:

Von Neumann is an old computer architecture based on a stored program computer system with the same physical memory address utilized for instruction and data. There is a common bus for the transport of instructions and data. As a result, it's less expensive than Harvard Architecture. Because its CPU cannot access instructions while reading or writing, it is mostly utilized in personal and tiny computers.

A contemporary computer architecture called Harvard Architecture is based on the Harvard Mark I relay-based paradigm and has separate physical memory for storing instructions and data. Due to the utilization of separate buses for data and instruction transfer, it may complete all of its instructions in a single cycle. In comparison to Neumann Architecture, it is more expensive since current technology is integrated. The major applications of this CPU are in micro controllers and signal processing since it can access instructions and read and write at the same time.

1. RISC vs CISC architecture:

RISC stands for Reduced Instruction Computer Processor. Since it requires multiple sets to store instructions, it stresses the software to optimize the instruction set. It is a programming unit that is hard-wired into the RISC processor, so it has simple decoding capabilities and simple path usage. Since it has more transistors on the memory registers, the execution time of RISC is very short  
CISC stands for Complex Instruction Computer. It is a firmware unit where it emphasizes the hardware to optimize the instruction set. Since it contains a single set of registers to store instructions, it has complex decoding instructions and difficult path usage compared to CISC. The execution time is very long because it uses load and store instructions in the memory-to-memory interaction of a program.